Design and Analysis of Novel High-Gain and Broad-Band GaAs pHEMT MMIC Distributed Amplifiers With Traveling-Wave Gain Stages

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***Abstract*—Using the concept of traveling-wave gain stages, novel GaAs pseudomorphic high electron-mobility transistor monolithic-microwave integrated-circuit (MMIC) distributed amplifiers (DAs) are demonstrated to achieve high gain and over several octaves of bandwidth performance simultaneously for microwave and millimeter-wave frequency applications. The cascaded single-stage distributed amplifier (CSSDA) is used as traveling-wave gain stages to improve the gain performance of the conventional distributed amplifier (CDA). By adopting the low-pass filter topology between the CDA and CSSDA and tuning the gain shape of CDA and CSSDA separately, a broad-band and high-gain DA, called CDA–CSSDA-2, was accomplished. The detailed design equations are derived for the broad-band matching design of this CDA–CSSDA-2. Two other MMICs, namely, a two-stage CSSDA called 2-CSSDA, and another two-stage design called CDA–CSSDA-1, are also included in this paper. This CDA–CSSDA-2 achieves 22±1.5-dB small-signal gain from 0.1 to 40 GHz with a chip size of 1.5 × 2 mm^2. It also produces a gain-bandwidth product of 503 GHz, which is the highest among all reported GaAs-based DAs. The flat group delay also demonstrates the feasibility of this design for future digital optical communications and broad-band pulse applications.**

***Index Terms*—Broad-band, cascaded single-stage distributed amplifier (CSSDA), conventional distributed amplifier (CDA), distributed amplifier (DA), monolithic microwave integrated circuit (MMIC), traveling-wave gain stage.**

I. Introduction

THE principles of the broad-band capability of distributed amplifiers (DAs) are well known [1]–[3]. The advantages of uniform gain, flat group delay, and low voltage standing-wave ratio (VSWR) over wide frequency ranges in DAs have also made it possible to implement a broad-band millimeter-wave receiver for digital optical communications [4]–[8] and other pulse applications. In addition to the conventional common-source topology to implement DAs, there were many other reported circuit topologies to implement high-performance DAs for digital optical communications, such as cascode [3], [4], [8], [10], dual-gate [11], matrix [12], differential [5], [13], attenuation compensation [14], twin-cascode [5], and cascade [9], [15]–[17] using GaAs, InP, SiGe, GaN, and CMOS foundry processes. However, the performances of the conventional distributed amplifier (CDA) are gain-bandwidth limited due to its optimum number of stages [2]. The cascode configuration (a common-source field-effect transistor (FET) connected with a common-gate FET) DA, known for its high maximum available gain, wide bandwidth, improved input–output isolation, and variable gain control capability, has been utilized in many applications such as distributed mixers [18]–[20], and DAs [3], [4], [8], [10]. To make a very compact monolithic microwave integrated circuit (MMIC) DA design possible, the cascode FET gain cell are sometimes realized as a dual-gate structure. However, the dc power consumption of the cascode DA is higher since the dc voltage across the cascode cell is doubled as in the CDA and also the dc current flows through the drain and gate termination resistors. The differential and twin-cascode DAs are promising topologies to obtain better gain performance and are less noisy than that of the CDA, but the chip size and dc power consumption are of concern. The attenuation compensation technique used in the DA design could reduce the gate- and drain-line transmission losses and enhanced the gain performance in the high-frequency band, but the stability in the high frequency and chip size will be issues. The cascaded single-stage distributed amplifier (CSSDA), unlike the CDA, does not need to equalize the phase velocity on the gate and drain lines, but still needs to match the characteristic impedance of inter-stage transmission lines. The CSSDA shows excellent performance with high gain, good gain flatness, lower input and output VSWRs, flat group delays, and a low noise figure.

Using a more advanced MMIC process, the DAs fabricated on InP substrates [7]–[10] have achieved higher gain-bandwidth products (GBWs) than those fabricated on GaAs [4]–[6], [13], [14], [21], [22]. In order to obtain high-gain performance, it is useful to cascade two identical DAs or using the twin cascode methodology [5], but the chip size and dc power consumption will also be increased. In this study, by adopting the proposed circuit topology on the GaAs substrates, a novel broad-band MMIC DA has been designed and demonstrates the GBW of 503 GHz, which could be comparable with those of DAs using an InP-based high electron-mobility transistor (HEMT) MMIC process.

There are several DA designs that tried to add gain stages to improve gain/power capabilities, but most of their gain performances result in bandpass shape [23]–[25], not as the full-band shape in CDAs, and these broad-band amplifiers are band

Manuscript received April 17, 2003; revised June 24, 2003. This work was supported in part by the National Science Council of Taiwan, R.O.C., under Project NSC 90-2219-E-002-007 and Project NSC 89-2213-E-002-178 and by the Ministry of Education, R.O.C., under Research Excellence Program ME 89-E-FA06-2-4.

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Digital Object Identifier 10.1109/TMTT.2003.818583

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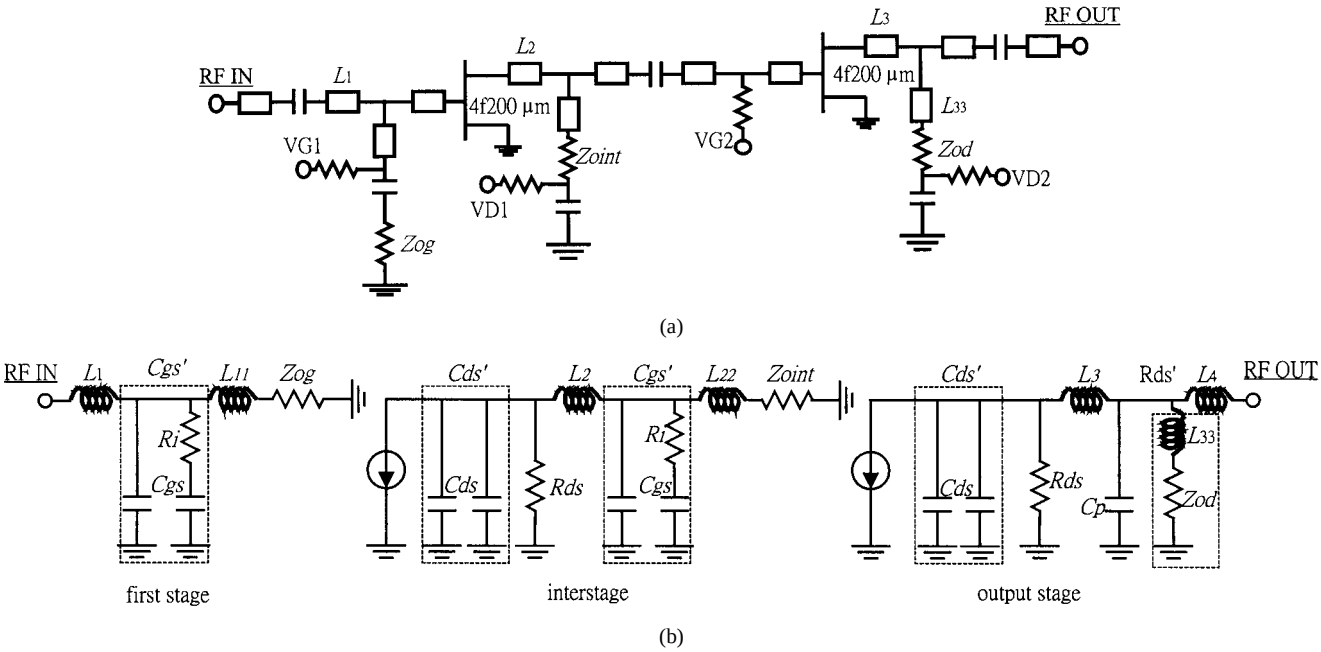


Fig. 1. (a) Schematic diagram of the 2-CSSDA $(n = 2)$. (b) Small-signal equivalent circuit of the 2-CSSDA. The capacitances of the transmission line are also considered in the equivalent circuit.

limited. By using the concept of traveling-wave gain stages to maintain the DA broad-band performance, the CSSDAs [15], [16] are selected and designed as broad-band gain stages. This paper, for the first time, proposes a novel low-pass filter (LPF) topology to combine the CDA and CSSDA into a single chip, called the CDA–CSSDA-2, to achieve the high gain and wide bandwidth simultaneously $(\mathrm{GBW} = 503)$. For proof of concept, a two-stage cascaded single-stage DA (2-CSSDA) and CDA combined with one-/two-stage CSSDAs (i.e., CDA–CSSDA-1 and CDA–CSSDA-2) have been designed, fabricated, and tested. The 2-CSSDA shows band-limited performance, below 22 GHz. Adding a two-stage CDA in front of a one-stage CSSDA to form the CDA–CSSDA-1 can extend the bandwidth up to 27 GHz. Finally, a CDA–CSSDA-2 with a seven-stage CDA and two-stage CSSDA can provide high-gain (22 dB) and broad-band performance up to 40 GHz. The CDA–CSSDA-2 demonstrates wide-band high-gain with $\pm$1.5-dB ripple and flat group-delay performance, which also proves the feasibility of this approach for broad-band applications.

II. Device Characteristics and MMIC Fabrications

These MMIC DAs were fabricated using a GaAs-based pseudomorphic high electron-mobility transistor (pHEMT) MMIC foundry process provided by TRW Inc., Redondo Beach, CA [26]. The active device is a 0.15-μm gate-length pHEMT with a unit current gain frequency (f_T) and a maximum oscillation frequency $(f_{\max})$ of 81 and 120 GHz. The peak of transconductance and maximum current at peak transconductance (I_{dsp}) are 400 mS/mm and 200 mA/mm, respectively. The passive components include GaAs thin-film resistors, metal–insulator–metal (MIM) capacitors, inductors, and via-holes through a 100-μm GaAs substrate. The entire chip is also protected by silicon–nitride passivation for reliability concern.

III. Circuit Design and Analysis

A. 2-CSSDA

The schematic representation and small-signal equivalent-circuit model of a two-cascaded single-stage distributed amplifier (2-CSSDA) is shown in Fig. 1. The transistor input and output capacitances (C_{gs} and C_{ds}) are absorbed into synthetic transmission lines (*LC* ladder networks) and the transmission-line equivalent capacitances are also considered in the circuit. These line sections are much shorter than a wavelength and can be modeled with an *LC* π-sections equivalent circuit. The bandwidth of the amplifier is then limited by the synthetic line cutoff frequency (f_c), the frequency-dependent losses associated with the transistor input and output capacitances (C_{gs} and C_{ds}), and the corresponding inductances of the artificial transmission lines, as shown in Fig. 1(b). The amplifier utilizes high-impedance artificial transmission lines in conjunction with active devices, which is composed of second-order wide-band LPFs. Each stages of the amplifier are formed by a T-section network. Compared with CDA, the 2-CSSDA demonstrates a significantly higher available gain [15] and improved gain flatness near cutoff frequency.

The forward available gain for a 2-CSSDA with a lossless transmission line is given by (1) and (2) [15], [16] as follows:

$$\mathrm{Gav}_{\mathrm{sgl}} = \frac{g_m^4 Z_{\mathrm{oint}}^2 Z_{og} Z_{od}}{4} \tag{1}$$

$$Z_{og} = \sqrt{\frac{L_1}{C'_{\mathrm{gs}}}}$$

$$Z_{\mathrm{oint}} = \sqrt{\frac{L_2}{C'_{\mathrm{ds}}}} = \sqrt{\frac{L_{22}}{C'_{\mathrm{gs}}}}$$

$$Z_{od} = \sqrt{\frac{L_3}{C'_{\mathrm{ds}}}} = \sqrt{\frac{L_4}{C_p}}. \tag{2}$$

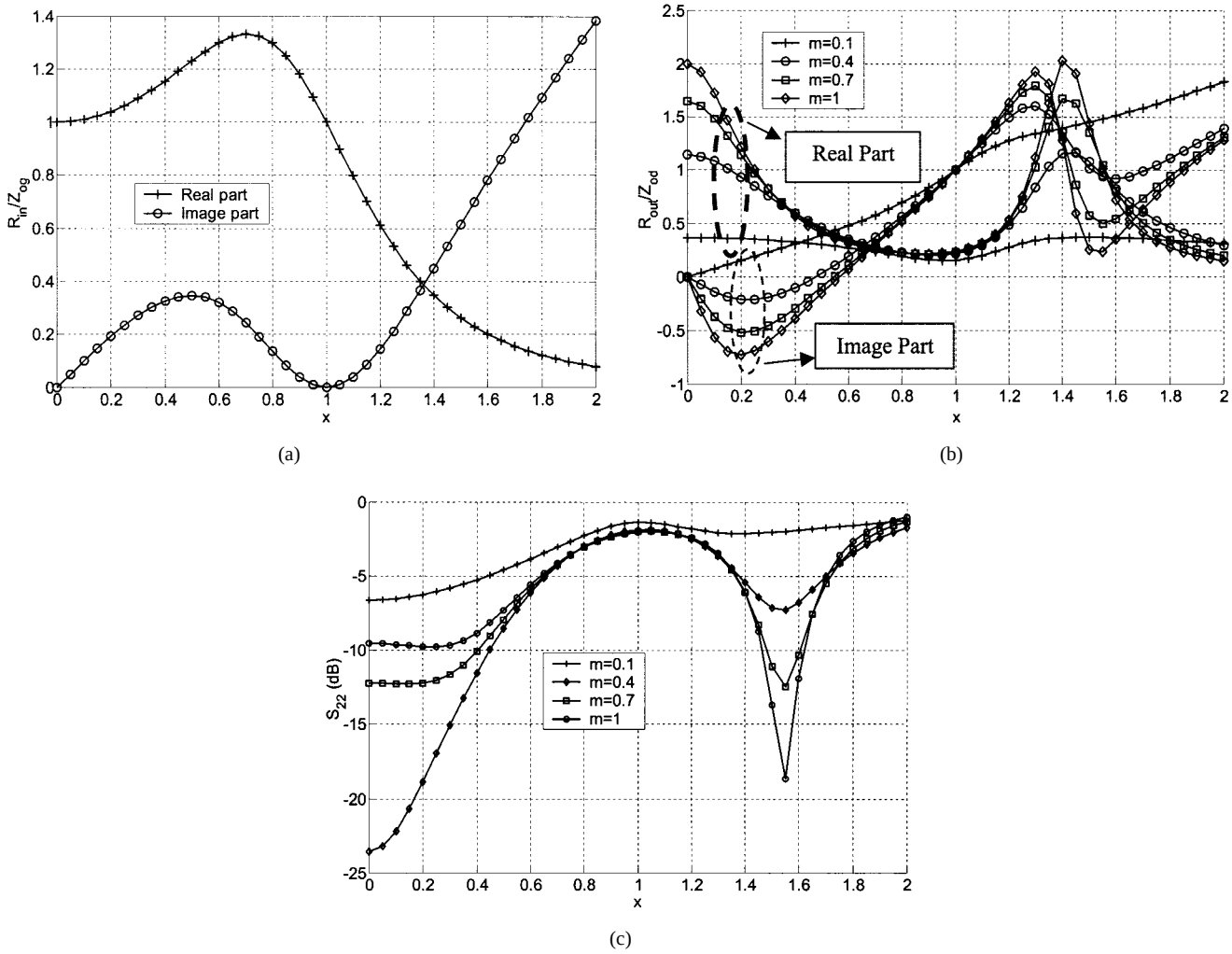


Fig. 2. Circuit simulation results of input and output impedances of the 2-CSSDA. (a) Real and image of input impedance. (b) Real and image of output impedance ($R_{\rm ds} = 200\ \Omega$). (c) Output return loss ($x = \omega/\omega_c$).

The high-gain performance can be significantly improved by increasing the number of stages. The input and output impedances of the 2-CSSDA are derived under the assumption of $L_1 = L_{11}$, $R_i \ll 1/(\omega C_{\rm gs})$, $L_3 = L_4$, $C'_{\rm ds} = C_p$, and $\omega L_{33} \ll X_{od}$, respectively, as follows:

$$Z_{\rm in} = Z_{og}\left[\frac{1}{1-x^2+x^4} + jx\frac{(1-x^2)^2}{1-x^2+x^4}\right] \tag{3}$$

$$Z_{\rm out} = Z_{od}\left[\frac{\left[b-x^2\left(3b+Z_{od}^2\right)+bx^4\right]+jxZ_{od}\left[R'_{\rm ds}+a(1-x^2)\right]}{aZ_{od}(1-x^2)+jx\left(2b-bx^2+Z_{od}^2\right)}\right] \tag{4}$$

$$\omega_c = \frac{1}{\sqrt{L_1 C'_{\rm gs}}} = \frac{1}{\sqrt{L_3 C'_{\rm ds}}} \tag{5}$$

where $x = \omega/\omega_c$ is the normalized frequency, $a = R_{\rm ds} + R'_{\rm ds}$; $b = R_{\rm ds} \cdot R'_{\rm ds}$, g_m is the transconductance of the active device, $Z_{\rm oint}$ is the inter-stage characteristic impedance, Z_{og} is the gate line characteristic impedance of the first stage, and Z_{od} is the drain line characteristic impedance of the last stage.

In low-frequency approximation, the input and output impedances can be simplified as

$$Z_{\rm in} \cong Z_{og} + j2\pi f(L_1 + L_{11}), \quad \text{if } s^2 C'_{\rm gs} L_{11} + sC'_{\rm gs} Z_{og} \ll 1 \tag{6}$$

$$Z_{\rm out} \cong Z_{od} + j2\pi f(L_{33} + L_4), \quad \text{if } s^2 C'_{\rm ds}(L_{33} + L_3) + sC'_{\rm ds} Z_{od} \ll 1 \tag{7}$$

where $s = j2\pi f$. In the low frequency, the Z_{og} and Z_{od} termination resistors would dominate return losses and the real part of the input impedance is bigger than the image part, as shown in Fig. 2(a), which means the input matching is easy to obtain under cutoff frequency ($x = 1$). However, above the cutoff frequency (ω_c), due to the transmission-line effect, the imaginary part of the input impedance will dominate so it is difficult to get good input impedance matching in high frequency for the 2-CSSDA. On the contrary, the imaginary part of the output impedance is comparable to the real part, as shown in Fig. 2(b), which means more design efforts on the

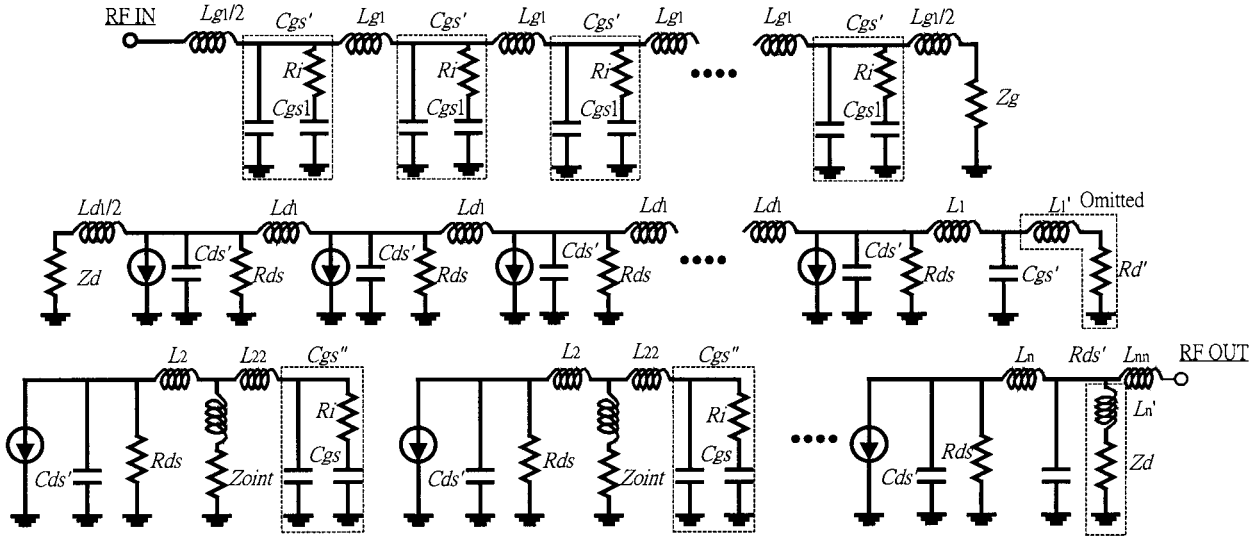
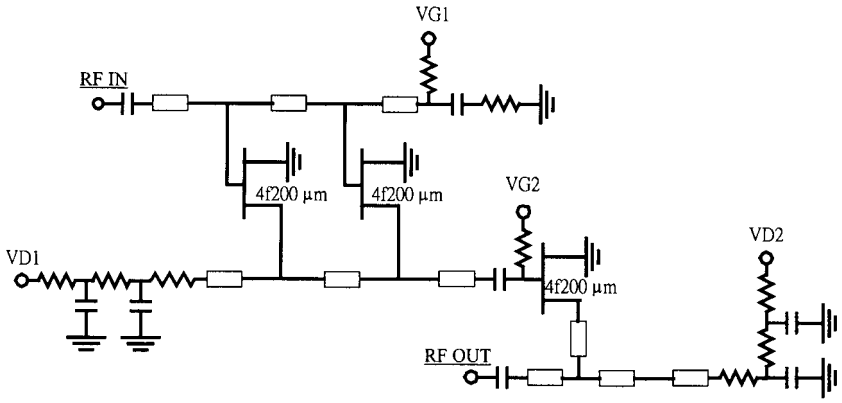
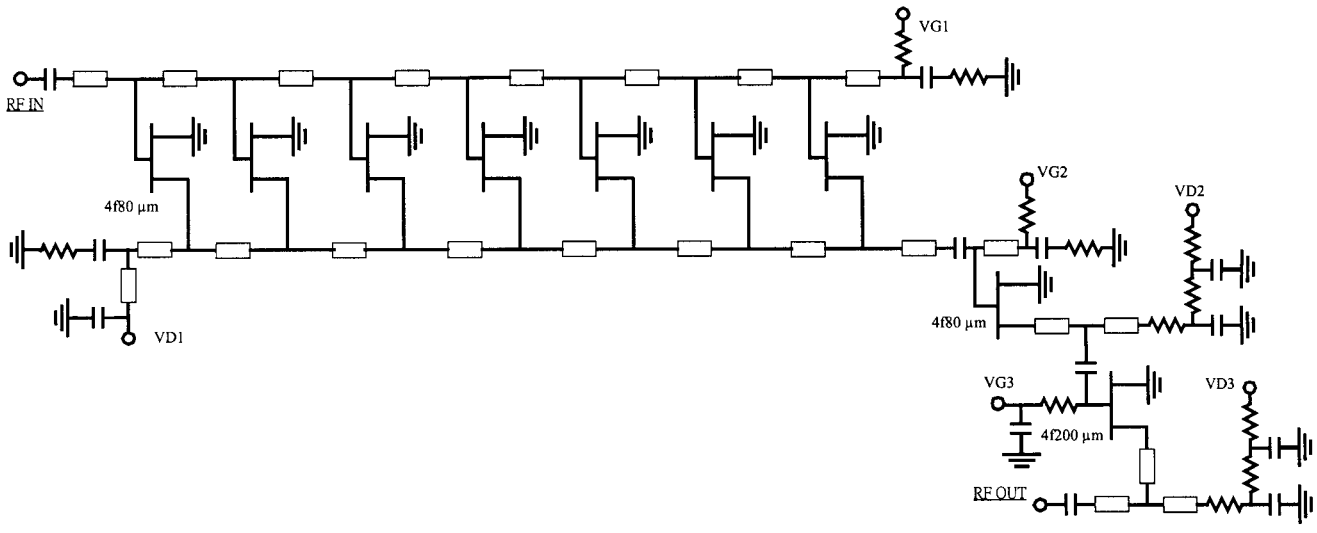


Fig. 3. Small-signal equivalent circuit of the proposed traveling-wave amplifier approximates an equivalent *LC* model. The first two rows represent the gate/drain transmission line of the CDA with the input stage of the CSSDA as the drain line end. The third row represents the equivalent-circuit model of the CSSDA.



(a)

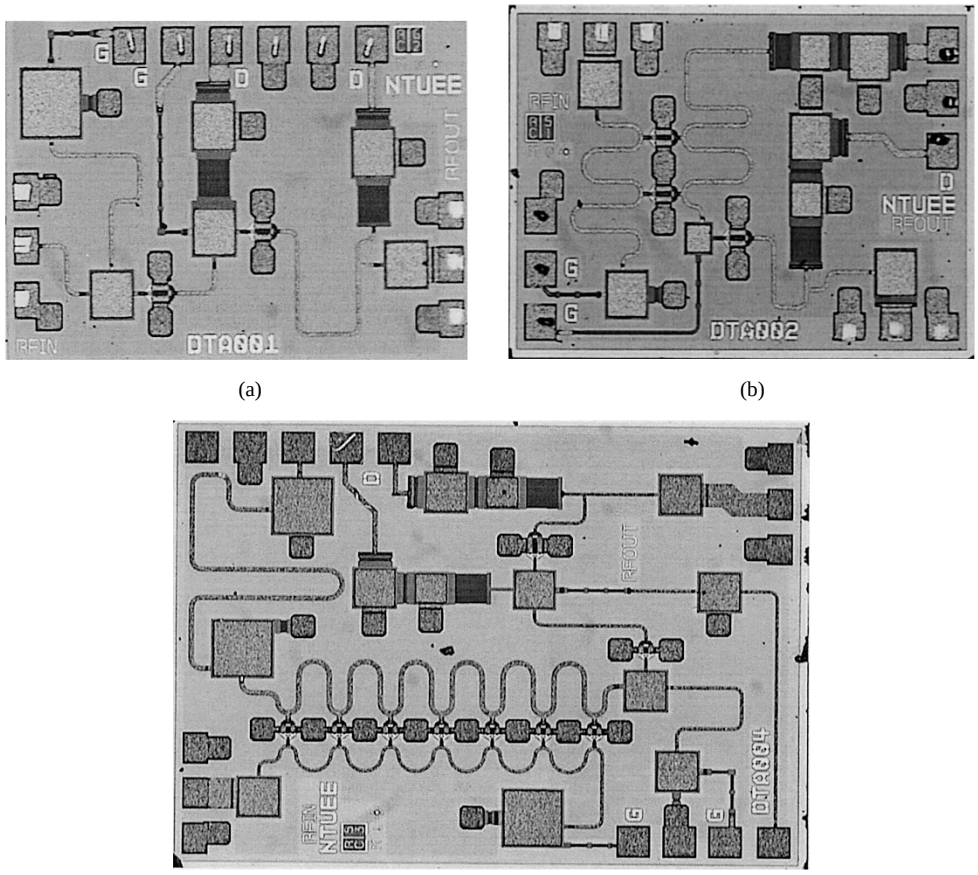


(b)

Fig. 4. Schematic diagrams of the new proposed broad-band MMIC DAs. (a) CDA–CSSDA-1. (b) CDA–CSSDA-2.

CSSDA output matching than on the input port. It is assumed that $m = R'_{\rm ds}/R_{\rm ds}$ so $Z_{\rm out}$ can be also expressed as (8), shown at bottom of the following page.

By selecting the proper m value and $R_{\rm ds}$ of the HEMT, one could get good output impedance matching below the cutoff frequency of the synthetic transmission line, as shown



(a) (b)

(c)

Fig. 5. Chip photographs of the broad-band: (a) 2-CSSDA, (b) CDA–CSSDA-1, and (c) CDA–CSSDA-2 with a die size of 1.5 × 1 mm^2, 1.5 × 1 mm^2, and 1.5 × 2 mm^2, respectively.

in Fig. 2(b) and (c). For higher m, the output return loss S_{22} will be decreased, but the high $R'_{\rm ds}/R_{\rm ds}$ ratio is difficult to realize. In this design, the four-finger 80-μm device has $R_{\rm ds}$ of 515.6 Ω $(m = m_1 = 0.233)$ for the first stage, and the four-finger 200-μm device has $R_{\rm ds}$ of 296.54 Ω $(m = m_2 = 0.4)$ for the second stage. Above the cutoff frequency, due to the transmission-line effect, the output port return loss will be degraded.

The input and output stages of CSSDA are designed to match to the 50-Ω environments. To maintain the broad-band matching, the input/output matching can be realized through equalizing capacitor value as

$$C'_{\rm gs} = C'_{\rm ds} = C_p. \tag{9}$$

Other than at these two ports, all the linewidths of the transmission lines are the same with different lengths to achieve an optimal overall performance.

B. CDA–CSSDA-1 and CDA–CSSDA-2

The forward available gain $\mathrm{Gav_{con}}$ of a CDA for a lossless m-stage amplifier is given [1]–[3] as follows:

$$\mathrm{Gav_{con}} = \frac{m^2 g_m^2 Z_d Z_g}{4} \tag{10}$$

where m is the number of stages of the CDA, g_m is the transconductance of the active device, and Z_d and Z_g are the characteristic impedance of the drain and gate lines, respectively. In the CDA configurations, there will be a cutoff frequency limited by both the gate and drain capacitances ($C_{\rm gs}$ and $C_{\rm ds}$) and the corresponding inductances of the artificial transmission lines. Therefore, $\mathrm{Gav_{con}}$ of the CDA is limited to 7–14 dB [15], which is due to the fact that the configuration of the CDA is fixed to an optimum number of active devices, i.e., four or five for hybrid and six or eight for monolithic technologies [29], and there is also a instability problem as the frequency approaching the cutoff frequency of the gate or drain transmission lines.

Due to the second-order LPF configuration, the bandwidth of the 2-CSSDA is band limited compared with the CDA. The

$$Z_{\rm out} = Z_{od}\left[\frac{\left[mR_{\rm ds}^2 - x^2\left(3mR_{\rm ds}^2 + Z_{od}^2\right) + mR_{\rm ds}^2 x^4\right] + jxZ_{od}\left[mR_{\rm ds} + (1+m)R_{\rm ds}(1-x^2)\right]}{(1+m)R_{\rm ds}Z_{od}(1-x^2) + jx\left(2mR_{\rm ds}^2 - mR_{\rm ds}^2 x^2 + Z_{od}^2\right)}\right] \tag{8}$$

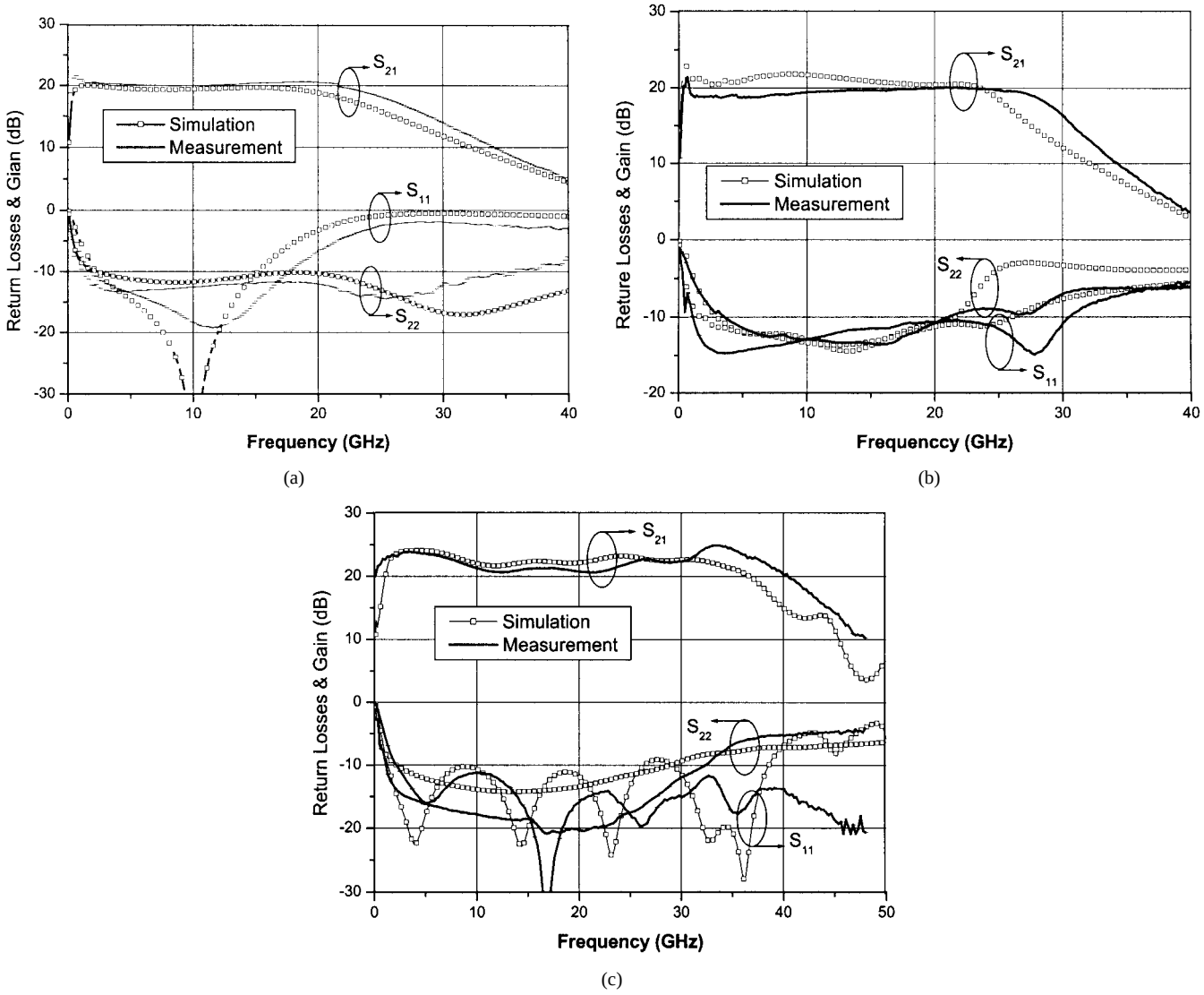


Fig. 6. Simulation results of the small-signal performance of the novel broad-band MMIC DAs. (a) 2-CSSDA. (b) CDA–CSSDA-1. (c) CDA–CSSDA-2.

simulation results of the 2-CSSDA show a limited bandwidth (below 22 GHz). As the number of stages of the amplifier increases, the low-frequency gain also increases so it is not easy to design a flat gain performance for a multistage CSSDA.

Therefore, the novel methodology for broad-band MMIC DAs, which combined the CDA used to extend wider bandwidth and CSSDA/2–CSSDA as a gain stage, is proposed to operate at a high gain and over several octaves of bandwidth simultaneously. The small-signal equivalent circuit is shown in Fig. 3 with the m-stage CDA cascaded n-stage CSSDA. In this proposed MMIC DA, the CDA is used in the first stage and the design methodology of the CDA is the same as the CDA [1]–[3]. Thus, the amplified forward signal in the CDA output will go through the LPF, part of the signal will travel down to the CSSDA, and the others will be absorbed by the termination resistor $R'_{\rm ds}$, as shown in Fig. 3. The LPF topology is adopted between the CDA and CSSDA and by tuning the gain shape of the CDA and CSSDA and, thus, the broad-band and high-gain performances are obtained. To cover the same bandwidth as the drain line in the CDA, the device size of first stage in the CSSDA is selected as the same size as in the CDA. The device size in the second stage is approximately twice that as in the first stage for output power consideration. The CSSDA design follows the previous design (1)–(9).

The forward available gain Gav_n of the proposed DA for combining the m-stage CDA and n-stage CSSDA is given as

$$\mathrm{Gav}_n = \frac{m^2 g_m^2 Z_d Z_g}{4} \cdot \frac{g_m^{2n} Z_{oint}^{2(n-1)} Z_{od} Z_{og}}{4}. \qquad (11)$$

This proposed amplifier overcomes the drawbacks of the CDA and CSSDA because of the following reasons.

1) The CDA is used as the first stage, extended the bandwidth; the input VSWR of the proposed DA is low over a very wide-band frequency.
2) There is also no stability problem as the frequency approaches the cutoff frequency of the gate or drain line due to the control of the length of the transmission line between the CDA and CSSDA and the capacitor $C_{\rm gs}$ of the first stage of the CSSDA, which is absorbed into the artificial transmission line of the drain line of the CDA and is composed of a broad-band LPF. The shunt capacitor $C_{\rm gs}$ can be optimized through the device size selections.

3) Tuning the gain shape of the CDA and CSSDA can control the gain flatness of the proposed DA; extend to low frequency range.
4) The number of devices, dc power consumption, and chip size are less compared with the method of using the cascade two DAs and twin cascade DA.

C. MMIC Design and Simulation

The linear pHEMT model used in the simulation is provided by the foundry and is implemented in the commercial computer-aided design (CAD) software (LIBRA from HP-EESOF). In order to demonstrate the concepts of the proposed DAs, three types of DAs, i.e., 2-CSSDA, CDA–CSSDA-1, and CDA–CSSDA-2, are designed. The schematic diagrams of the proposed DAs are shown in Figs. 1(a) and 4. The chip photographs of these broad-band DAs are shown in Fig. 5. In Fig. 1(a), the 2-CSSDA is designed. The port return losses of linear simulation results for the amplifier are better than -5 dB and small-signal gain of 19 ± 1 dB in the desire frequency band are shown in Fig. 6(a) and the bandwidth is limited. Fig. 5(a) shows the chip photograph of the MMIC with a die size of 1.5×1 mm^2. In Fig. 4(a), the two-stage CDA cascaded with the one-stage CSSDA (CDA–CSSDA-1, $m = 2$, $n = 1$) is designed. The port return losses of linear simulation results for the amplifier better than -8 dB and small-signal gain of 19 ± 1 dB in the desired frequency band are shown in Fig. 6(b). Compared with the input return loss of the 2-CSSDA, the CDA–CSSDA-1 can obtain better return loss due to use of the CDA in the first stage. Fig. 5(b) shows the chip photograph of the MMIC with a die size of 1.5×1 mm^2. In order to demonstrate the concepts for millimeter-wave application, the CDA–CSSDA-2 is also designed ($m = 7$, $n = 2$), as shown in Fig. 4(b). The port return losses of linear simulation results for the amplifier better than -8 dB and small-signal gain of 22 ± 1 dB in the desired frequency band are shown in Fig. 6(c). The CDA–CSSDA-2 can obtain better return loss due to use of the CDA in the first stage. Fig. 5(c) shows the chip photograph of the MMIC with a die size of 1.5×2 mm^2.

The stability is a very important issue in the DA design especially as the frequency approaching the cutoff frequency of the synthetic transmission line. The K factor of the complete CDA–CSSDA-2 is greater than one. The CDA–CSSDA-2 was separated into two sub-circuits (CDA and CSSDA) and the individual K factors and small-signal gain performance were both inspected. It was observed that, as the frequency approaches to the cutoff frequency of the gate and drain synthetic transmission lines, the circuit K factors of CSSDA-2 and CDA will be lower than one. By checking the loop-oscillation condition [27] in the CDA and the inter-stage stability circles between the CDA and CSSDA, there is no stability problem in the complete circuit CDA–CSSDA-2. This stability improvement is due to that we can control the cutoff frequency of the synthetic transmission line between the CDA and CSSDA by adjusting the length transmission line and input capacitance (C_{gs}) of the CSSDA.

IV. Circuit Performance

The three MMIC DAs, i.e., 2-CSSDA, CDA–CSSDA-1, and CDA–CSSDA-2, were all measured via on-wafer probing. The

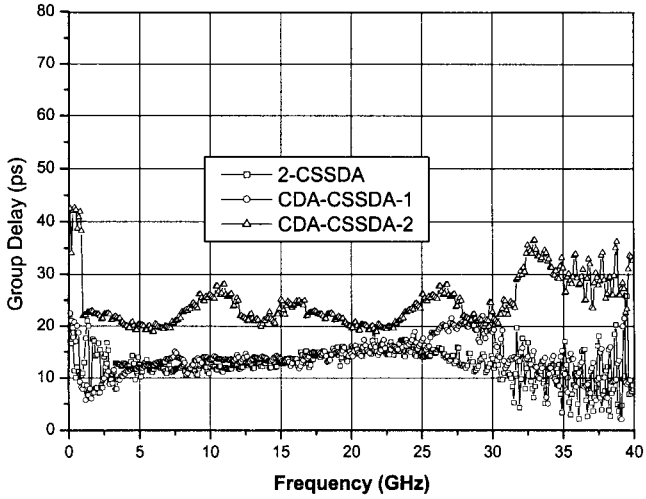


Fig. 7. Measured group delay of the proposed broad-band MMIC DA (2-CSSDA, CDA–CSSDA-1, and CDA–CSSDA-2).

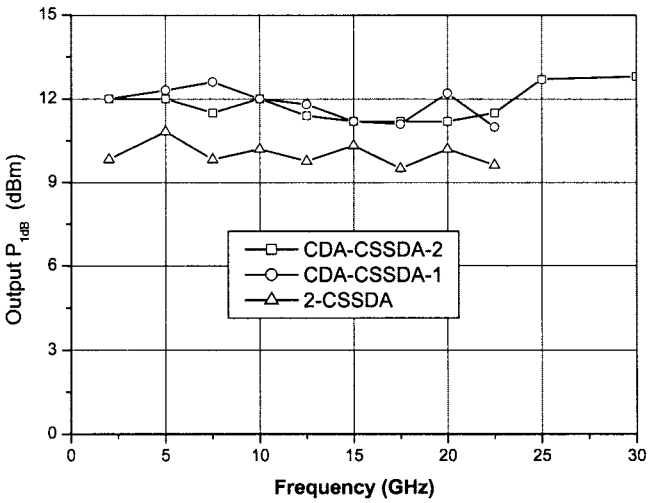


Fig. 8. Measurement results of the output P_{1dB} of these novel broad-band MMIC DAs. (2-CSSDA, CDA–CSSDA-1, and CDA–CSSDA-2).

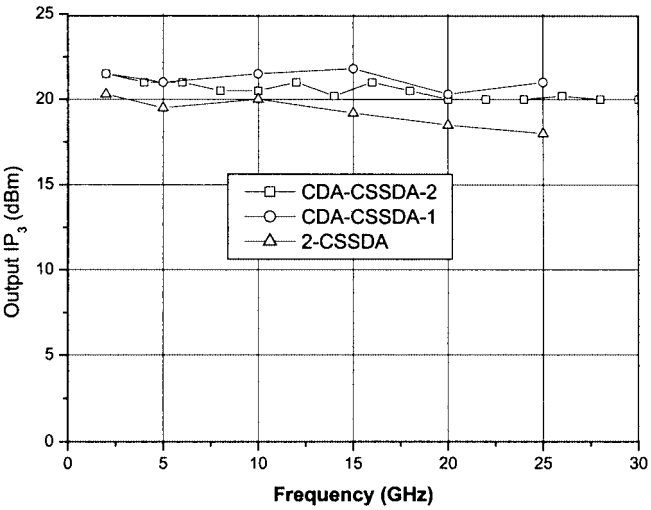


Fig. 9. Measurement results of the output IP_3 versus input frequency of these novel broad-band MMIC DAs (2-CSSDA, CDA-CSSDA01, and CDA–CSSDA-2).

TABLE I
SUMMARY OF THE PREVIOUSLY PUBLISHED DISTRIBUTED AMPLIFIERS AND THIS STUDY

Freq. (GHz)	Gain(dB)	GBW (GHz)	Design Features	Chip Size (mm^2)	Ref.
0.1-54	15	303	GaAs 0.15 μm HEMT, cascade, GCPW design, 8 stages	2.7x2.2	[4]
0.1-46	20	460	GaAs 0.15 μm PHEMT, twin cascode, CPW design, 8 stages	1.5x4	[5]
0.1-65	14.5	345	GaAs 0.15 μm MHEMT, cascode, ML design, 7 stages	1.4x1.2	[6]
1-50	24	792	InP 0.1 μm HEMT, cascade, CPW design, 4 stages		[7]
0.1-70	17	495	InP D-HBT, attenuation compensation, CPW design, 7 stages	0.6x1.8	[8]
0.1-92	12.5	387	InP S-HBT, cascode, CPW design, 5 stages	1.6x0.4	[8]
0.1-70	17	495	InP 0.1 μm HEMT, cascade, CPW design, 3 stages		[9]
0.1-92	13	410	InP 0.1 μm HEMT, cascade, CPW design, 10 stages	2.5x1.2	[10]
0.1-40	22	503	GaAs 0.15 μm PHEMT, ML design, (CDA-CSSDA-2)	1.5x2	This work
0.5-27	19	236	GaAs 0.15 μm PHEMT, ML design, (CDA-CSSDA-1)	1.5x1	This work
0.5-22	20	215	GaAs 0.15 μm PHEMT, ML design, (2-CSSDA)	1.5x1	This work

small-signal characteristics, output P_{1dB}, group delays, and output IP_3 were evaluated. Fig. 6(a) shows small-signal gain of 20 dB with flatness ± 1 dB and port return losses better than -5 dB for the 2-CSSDA in the frequency range of 0.5–22 GHz with total dc power consumption of 180 mW. Due to selecting the optimal m value and R_{ds} of the device, the output port return loss is better than -10 dB in high frequency. For the CDA–CSSDA-1, the measured small-signal gain is 19 ± 1 dB and port return losses are better than -8 dB in the frequency range of 0.5–27 GHz, as shown in Fig. 6(b), with total dc power consumption of 324 mW. It is also observed that by using the CDA in the first stage of the DA, the input port return loss is better than the 2-CSSDA. For the CDA–CSSDA-2, the measured small-signal gain is 22 ± 1.5 dB and port return losses are better than -5 dB in the frequency range of 0.1–40 GHz, as shown in Fig. 6(c), with total dc power consumption of 484 mW. The measurement results agree well with the simulation results. It is noted that the gain rolloff of these amplifiers are very gradual. This is because the sharp gain rolloff, which is often observed in DAs, will lead to excessive group delay peaking and a deteriorated eye diagram [5]. Fig. 7 shows the average group delay 30 ± 10 ps of the CDA–CSSDA-2 and 12 ± 5 ps of the 2-CSSDA and CDA–CSSDA-1. The flat group delay of the proposed DA is very important for digital optical communications. The output P_{1dB} of all three DAs from 2 to 30 GHz are shown in Fig. 8, which shows the output P_{1dB} of 10, 11.5, and 12 dB for 2-CSSDA, CDA–CSSDA-1, and CDA–CSSDA-2, respectively. The output IP_3 versus input frequency of all three DAs are also presented in Fig. 9. The output IP_3 of 18–20 dB for the 2-CSSDA and 22–20 dB for the CDA–CSSDA-1 in the frequency range of 2–25 GHz is obtained. It is observed the output IP_3 of CDA–CSSDA-1 is higher than the 2-CSSDA 2 dB in high frequency. The output IP_3 is 22–20 dB in the frequency range of 2–30 GHz for the CDA–CSSDA-2 and operated at 30 GHz also demonstrates the power gain of 22 dB for the RF input power level lower than -10 dBm.

Considering the dc power consumption issue, a GaAs pHEMT cascode DA [28] with eight stages and a total of 1280-μm device periphery shows 15-dB gain up to 40 GHz and dc bias at 7 V and 180 mA. Compared with the CDA–CSSDA-2 in this paper, we can achieve 40-GHz bandwidth with half dc power consumption (484 mW) and much higher gain (22 dB).

Table I summarized the features and performances of the previously published DAs and this study. Compared with the previously published results [4]–[9], this MMIC CDA–CSSDA-2 demonstrated the highest GBW performance among these MMICs using GaAs-based HEMTs and are also comparable with those DAs using InP-based HEMT technologies.

V. CONCLUSION

This paper presented the novel high-gain and broad-band MMIC DAs, which combined a CDA and CSSDA. The distributed amplifier (CDA–CSSDA-2) produces a GBW of 503 GHz, which is significantly higher than GaAs-based DAs. By selecting the LPF topology between the CDA and CSSDA and tuning the gain shape of the CDA and CSSDA separately, the broad-band performances are obtained. The detailed design equations are derived for the broad-band matching design of this CDA–CSSDA-2. To verify the design equations, two other MMICs, i.e., a two-stage CSSDA and two-stage CDA–CSSDA-1, are also included in this paper. The number of devices, dc power consumption, and chip size are less compared with the method of using the cascade two DAs and twin-cascade DA. The flat group delay performance also proves the feasibility of this approach, which is suitable for digital optical communication and broad-band pulse applications.

ACKNOWLEDGMENT

The MMIC foundry service was provided by TRW through the Chip Implementation Center (CIC), Taiwan, R.O.C. The authors would like to thank Dr. Y.-Z. Juang, CIC, for the foundry service coordinate effort.

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